Linear Current Division Principles

Haibo Fei, Randy Geiger
Electrical and Computer Engineering
Iowa State University
Ames, IA 50011 U.S.A
haibofei@iastate.edu

***Abstract*—this paper presents the study of a well established linear current division circuit, which has been referenced many times in published works as a basic building block in variety applications up to date. Understanding the advantages and, even more important, the limitations of this technique would benefit the further exploiting of potential applications. Analytic study with close form expressions shows highly agreements with the original statement that this structure is inherently linear and the linearity is independent of the electrical variables and only relies on the transistors geometrical match performance. However, the more accurate study with simulation results suggests that there are limitations for using this technique in terms of high linearity in the most popular semiconductor processes. Thereby more general circuit principles behind reported high linearity is of particular interested.**

I. INTRODUCTION

A standard current divider circuit is shown in Fig. 1a. In this current divider, part of the input current passes through one subcircuit and the balance passes through a second subcircuit. If ideal, it will provide a branch current in one subcircuit, I_1, which is a fixed fraction of the total input current, I_{IN}. In this case, the branch current can be expressed as

$$I_1 = \theta I_{IN}, \tag{1}$$

where θ is independent of I_{IN} or any other electrical variables in the circuit. Accurate and linear current division circuits are widely required in the design of data converters, analog filters and a host of other applications. The most basic current divider circuit is that obtained by replacing C_{kt1} and C_{kt2} in Fig. 1a with resistors.

Circuits that have some of the properties of the basic current divider have also been called "current dividers" [1] although the exact definition of more general current dividers are not well-established. Two circuit structures that share some of the same properties of the basic current divider are shown in Fig. 1b and Fig. 1c. In the more general current divider of Fig. 1b, it may not be possible to partition the current divider into two distinct subcircuits but the partitioned sourcing currents entering the current divider will remain as partitioned sinking current exiting the current divider as shown in the figure. In an even more general current divider, the partitioned sourcing currents may not be available as sinking currents. This situation is depicted in Fig. 1c. In this paper, the definition of "current divider" will be relaxed defined.

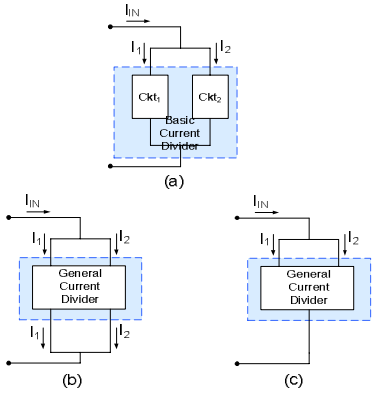

Figure 1. General Format of Current Divider

In 1992 Bult and Geelen [1] introduced an interesting and simple two-transistor current divider that was claimed to be "inherently linear" with a current division factor that is dependent only upon the devices geometries. In addition to its small size, the authors observe that this divider is attractive because the attenuation factor can be accurately controlled in most semiconductor processes and because the full-scale input is large essentially extending to the level that will cause either one of two transistors to enter the weak inversion of operation. The Bult-Geelen circuit, presented in [1], is shown in Fig.2.

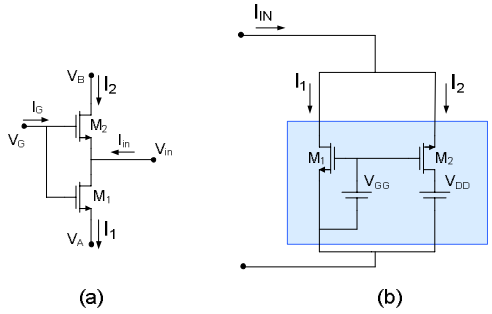

Figure 2. Inherently Linear Current Divider [1]

This structure has been influential in the development of the digitally programming current division block used in MOSFET-only ADC converter [2],a baseband channel-select filter for multi-standard

wireless receiver [3], digitally tuning analog filters [4], variable gain current amplifier [5], and several other applications [6]-[7].

The reported linearity performance based on this current divider was phenomenal; the THD of a volume control circuitry [1] was better than -85 dB, the THD of a 10-bit A/D [2] converter was -79dB, and a channel-select filter [3] built around this structure achieved -80~-94 dB spurious free dynamic range (SFDR). These linearity measures, all experimentally verified, are very impressive considering that the critical parts of these circuits are derived from small MOS transistors configured as simple two-transistor current dividers rather than with large passive components. It is then particular interesting to explore the benefits and limitations of this technique for further improving its linearity.

However, the following study presented in this paper will demonstrate that this Bult-Geelen current divider didn't exploit the linearity of this current divide circuit or the properties of this two transistor current divider but rather exploit somehow more general electrical circuit principles.

An analytical study is going to be delivered in the following section and it will exhibit that the linearity with square-law model of this current division circuit is perfect.

II. Analytical Study of the Current Divider

Although this current divider has been reported with inherently high linearity, no analytical proves have been actually achieved. In this section, close form expression will be presented with square-law models for the MOS transistors.

The two-transistor current divider in Fig 2 can be looked as 4 terminals network. If the voltages of the terminals $\{V_{GA}, V_{BA}, V_{inA}\}$ have been chosen as the independent variables here, the ports currents $\{I_G, I_{IN}, I_1\}$ are naturally become dependent variables. It is easily to prove that two transistors can work in two different cases; M_1 and M_2 are both in the triode region or M_1 is operating in the triode region while M_2 is in the saturation region. If assume two transistors have the same threshold voltages and basic square-law models are used, for the first case, this 4-termianl circuit are modeled by (2)~(4):

$$I_G = 0, \tag{2}$$

$$I_1 = \eta_1\left(V_{GA} - V_T - \frac{V_{inA}}{2}\right)V_{inA}, \tag{3}$$

$$\begin{aligned} I_{in} = {} & \eta_1\left(V_{GA} - V_T - \frac{V_{inA}}{2}\right)V_{inA} \\ & - \eta_2\left(V_{Gin} - V_T - \frac{V_{BA} - V_{inA}}{2}\right)\left(V_{BA} - V_{inA}\right) \end{aligned}, \tag{4}$$

where, V_T is the threshold voltage, $\eta_1=\mu C_{OX}(W_1/L_1)$, and. $\eta_2=\mu C_{OX}(W_2/L_2)$. The branch voltages are defined as $V_{GA}=V_G-V_A$, $V_{BA}=V_B-V_A$, and $V_{inA}=V_{in}-V_A$. The current-divider properties are not apparent from this formulation.

If the mixed port variables $\{I_{in}, V_{GA}, V_{BA}\}$ are selected as the independent variables and thus $\{I_G, I_1, V_{inA}\}$ are the dependent variables, it follows from a tedious but straightforward analysis that the device can be equivalently modeled by (5)~(7);

$$I_G = 0, \tag{5}$$

$$I_1 = \left[\frac{\eta_1}{\eta_1 + \eta_2}\right]I_{in} + \frac{\eta_1\eta_2}{\eta_1 + \eta_2}V_{BA}\left(V_{GA} - V_T - \frac{V_{BA}}{2}\right), \tag{6}$$

$$V_{inA} = V_{GA} - V_T - \sqrt{(V_{GA} - V_T)^2 - 2\left(\left[\frac{1}{\eta_1 + \eta_2}\right]I_{in} + \frac{\eta_2}{\eta_1 + \eta_2}V_{BA}\left(V_{GA} - V_T - \frac{V_{BA}}{2}\right)\right)}. \tag{7}$$

Followed the similar derivation process, if M_1 works in the triode region and M_2 operates in the saturation region, the dependent variables $\{I_G, I_1, V_{inA}\}$ can be expressed as below:

$$I_G = 0, \tag{8}$$

$$I_1 = \left[\frac{\eta_1}{\eta_1 + \eta_2}\right]I_{in} + \frac{\eta_1\eta_2}{2(\eta_1 + \eta_2)}(V_{GA} - V_T)^2, \tag{9}$$

$$V_{inA} = (V_{GA} - V_T)\left(1 - \sqrt{\frac{\eta_1 - \frac{2I_{in}}{(V_{GA} - V_T)^2}}{\eta_1 - \eta_2}}\right). \tag{10}$$

The analysis can be expanded to the circuit comprised of any number of transistors and the general expression of the source current of the bottom transistor keeps the same format as shown in (6) and (9) and it will not be presented here due to the space limitation here.

From above formulas, this circuit can be considered as a current divider with general definition. The inherently linear current division property reported for this circuit is due to the linear dependence of I_1 on the current I_{in} of (6) and (9) in which the proportionality constant of the two-transistor current divider,

$$\theta_{TT} = \frac{\eta_1}{\eta_1 + \eta_2} \tag{11}$$

is unchanged as M_2 moves between the triode region and the saturation region of operation. The accuracy is determined by the inherent ratio matching potential of device dimensions in most semiconductor processes and can be seen by expressing θ_{TT} as

$$\theta_{TT} = \frac{\eta_1}{\eta_1 + \eta_2} = \frac{1}{1 + \left(\frac{L_1}{L_2}\right)\left(\frac{W_2}{W_1}\right)} \underset{L_1=L_2}{=} \frac{W_1}{W_1 + W_2}. \tag{12}$$

A comparison of (6) and (9) with the ideal current divider equation of (1) does show some significant differences as well. One distinction is that in whatever circuit this current divider is embedded, the voltages V_{GA} and V_{GB} must not depend upon I_{in} if the linear current division property is to be maintained. The second one is the presence of the term that is added to the I_{in} dependent term that serves as an offset. The third difference is the concern that unless the circuit is driven at the input node with a current source with infinite output impedance, the change in the voltage V_{inA} with I_{in} will cause the output impedance of the current source to modulate the current I_{in} thus introducing nonlinearity. If these conditions are appropriately managed, the current divider is perfectly linear and accurate in a process in which the simple square-law model accurately predicts the performance of the MOS transistor.

Unfortunately few if any processes in use today are accurately characterized by the simple square law model. As reported in [1], when a more accurate model is used, model-dependent nonlinearities will be introduced. An appreciation for the circuit performance and limitations as affected by a more accurate MOSFET model and an understanding of the limitations inherent in the architecture will now be developed. In particular, we will focus on accuracy and linearity of the current divider.

III. ACCURACY AND LINEARITY DEFINITIONS

Before more accurate model are used to explore the limitations of the linearity of this current divider, two coefficients would be established in the following part to evaluate this current divider fairly

A. Accuracy

From the expressions for I_1 in (6) and (9), the interest in the linear dependence of I_1 with I_{in}, the division factor of the current divider in the presence of a better device model will be defined as

$$\theta_{TTACT} = \left.\frac{\partial I_1}{\partial I_{in}}\right|_{\{I_{inQ}, V_{GAQ}, V_{inAQ}\}}, \qquad (13)$$

and the division factor accuracy, in percent, will be defined as

$$\gamma = \left[\frac{\theta_{TT} - \theta_{TTACT}}{\theta_{TT}}\right] \bullet 100\% \cdot \qquad (14)$$

B. Linearity

Two different definition of linearity will be resented here. One is based upon the deviation of the transfer characteristics of the attenuated current from a referenced straight line. Very similar with the definition of INL in data converter circuit, this linearity implies the linearity with the slow varying input signal. The second one is based upon the spectral performance of the output current in the presence of a sinusoidal excitation.

The fit line of the division factor will be defined as:

$$I_{1FIT}(I_{in}) = I_{1Q} + \left.\frac{\partial I_1}{\partial I_{in}}\right|_{\{I_{inQ}, V_{GAQ}, V_{inAQ}\}} \bullet (I_{in} - I_{inQ}), \qquad (15)$$

and the deviation, in percent, from the fit line will be defined as:

$$\Delta = \left[\frac{I_1(I_{in}) - I_{1FIT}(I_{in})}{I_{1FIT}(I_{in})}\right] \bullet 100\%, \qquad (16)$$

where I_{1Q} is the current I_1 at the quiescent value of the input current, I_{inQ}.

The spectral performance will be defined in terms of the total harmonic distortion (THD) of the time-varying part of I_1 in the presence of a sinusoidal input current. Both definitions of linearity are dependent upon the magnitude of the input current with the nonlinearity going to zero as the deviation of the input current from the quiescent value goes to zero. We will define a full-scale input current to be I_{1Q}/θ_{TT}. If the transistor M_2 is operating in the saturation region when I_{IN}=0, the full-scale input current will be the current that causes M_2 to leave strong inversion and represents the maximum input current for current divider. If the transistor M_2 is operating in the triode region, when I_{IN}=0, the full-scale input current does not represent an upper bound on the input current and can just be viewed as a reference current level.

IV. MORE ACCURATE ANALYSIS AND SIMULATION

Reminded from the section II, several simplifications have been made to achieve the final close form expressions and those simplifications, such as identical threshold voltages, ignoring the finite output impedance of the transistors, second order effects and the substrate effect, etc, are not valid in more accurate analysis. The performance of the current divider will now be considered with a more accurate model of devices used in current processes. An analytical analysis with a more accurate device model becomes unwieldy but a computer simulation is useful for developing an appreciation for the linearity and accuracy attainable with the current divider. Simulations will be based upon the circuit of Fig. 2b where the terminal voltages V_{DD} and V_{GG} are fixed. BSIM device models for the TSMC 0.35μ and the TSMC 0.18μ processes will be used for those simulations.

Characterizations for large devices and small devices, for large excess bias (V_{EB}=V_{GSQ}-V_T) and for small excess bias, for single-region and two-region operation of the transistors M_1 and M_2, and for large feature and small feature processes will be made.

The accuracy of an attenuator designed for an attenuation factor of θ_{TT}=0.5 for long devices is shown in Table 1.From this table it can be observed that the accuracy of the attenuation factor is quite limited unless the operation of both devices is restricted to the triode region when large excess bias voltages are used.

The linearity of this current divider will be verified with the similar strategy. Different sizes of the transistors, different bias level and different feature processes are simulated and simulation results are shown in Fig.3~Fig.6.

The static nonlinearity represented in forms of the deviation is shown in Fig.3 and Fig.4 for TSMC 0.35u process and TSMC 0.18 u process, respectively. In these plots, "TT" and "TS" represent the operation regions for M_1 and M_2, respectively. "TT" means M_1 and M_2 are both in triode region and "TS" represents one in triode while the other one in saturation. Also, HVeb and LVeb are the abbreviations of the terms "large excess bias voltage (overdrive voltage)" and "low excess bias voltage (overdrive voltage)".

TABLE I. ACCURACY OF CURRENT DIVIDER FOR DIFFERENT OPERATION REGION

V_{DD} (V)	V_{GG} (V)	V_{EB} (V)	W_1 (um)	W_2 (um)	L_1 (um)	L_2 (um)	Process	Q-Point Operation		θ_{TT}	θ_{TTACT}	γ (%)
								M1	M2			
1.1	1.1	0.23	12	12	4	4	0.35	Triode	Sat	0.5	0.476	**-4.8**
1.65	1.65	2.79	12	12	4	4	0.35	Triode	Sat	0.5	0.491	**-1.8**
0.2	1.2	0.303	12	12	4	4	0.35	Triode	Triode	0.5	0.491	**-1.8**
0.2	1.65	2.79	12	12	4	4	0.35	Triode	Triode	0.5	0.5	**0**
0.9	0.9	0.125	6	6	2	2	0.18	Triode	Sat	0.5	0.476	**-4.8**
1.8	1.8	1.34	6	6	2	2	0.18	Triode	Sat	0.5	0.483	**-3.4**
0.1	0.9	0.225	6	6	2	2	0.18	Triode	Triode	0.5	0.495	**-1**
1.8	1.8	0.898	6	6	2	2	0.18	Triode	Triode	0.5	0.493	**-1.4**

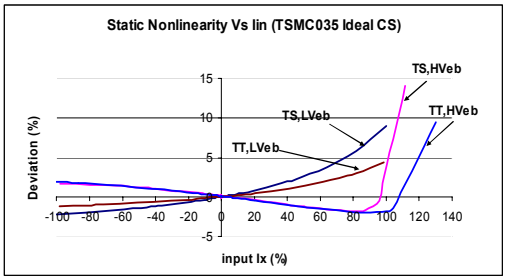

Figure 3. Static nonlinearity in TSMC035 process

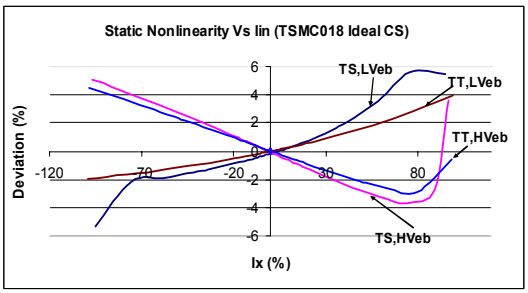

Figure 4. Static nonlinearity in TSMC018 process

From Fig.3 and Fig.4, it is clearly shown that the static linearity is very limited for even moderate magnitude of the input current with the notice that the deviation ranges from 3% to 5% when the input current approaching to about 50% of the full range. Also this static nonlinearity is dependent upon the biasing level and the operation regions of the transistors. One consistent phenomenon is that, in both two processes, the best linearity occurs when two transistors are both in the triode region with large V_{EB} voltage level. Recalling the best accuracy performance in the Table 1, it is very interesting to observe that the best accuracy can be obtained with two triode region operating transistors with large V_{EB} when static or dc linearity is required.

Another characteristic of the linearity for this current divider is the THD performance, which will represent the dynamic performance. The simulation results are shown in Fig. 5 and Fig.6.

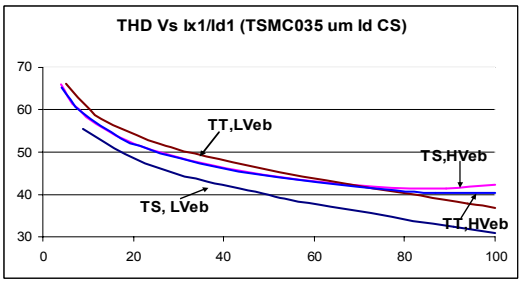

Figure 5. THD of the current divider for TSMC035 process

The THD performance again exhibits that the linearity of this current divider will limited to about 30~40 dB level if reasonable input current level is expected. The best linearity occurs when the two transistors are both in the triode region with low level V_{EB}. This is because the harmonic distortions are mainly due to the nonlinearity caused by the large input signal and the large V_{EB} will correspondingly require the larger input signal than small V_{EB} with the same percentage ratio.

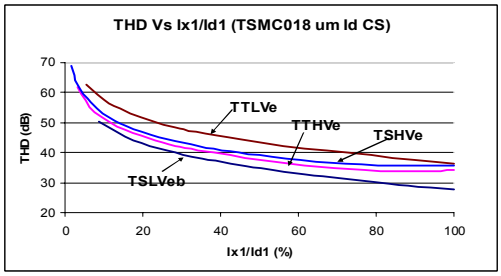

Figure 6. THD of the current divider for TSMC018 process

Although many others different simulations have been done to explore the linearity of this current divider including the minimum length devices, non-ideal input current sources and non-even current division ratios, the results will not be presented here due to the volume limitation. All the simulations exhibit the limited linearity with practical design models and also show the dependence of linearity upon the device size, biasing level, operation region and the processes technology.

V. Conclusion

A comprehensive study focusing on the linearity performance of a well-established simple current divider circuit has been presented in this paper. This work provides the first analytical close form approach which supports the statement about the linearity performance, and also demonstrates the potential benefit of this simple current divider for those applications with moderate linearity specifications. For low resolution applications, this technique is quite attractive for its simplicity and independency of electrical variables. The more accurate study with computer simulations exhibits the performance limitations of this technology and also shows the linearity dependence of all kinds of electrical variables. Thereby this study proves that the all the reported works with excellent linearity was actually based on more general circuit principles rather than the linearity of the current divider itself. Furthermore, this principle behind those works is of particular interested and study is undergoing.

References

[1] K. Bult and G.Geelen, "An Inherently Linear and Compact MOST-Only Current Division Technique", IEEE J. Solid-State Circuits, Vol. 26, pp. 1730-1735, Dec. 1992.

[2] C. Hammerschmied and Q. Huang, "Design and Implementation of an Untrimmer MOSFET-Only 10-Bit A/D Converter with -79dB THD", IEEE J. Solid-State Circuits, Vol. 33, pp. 1148-1157, Dec. 1992.

[3] H. Alzaher, H. Elwan and M. Ismail, "A CMOS Highly Linear Channel-Select Filter for 3G Multistandard Integrated Wireless Receivers", IEEE J. Solid State Circuits, Vol. 37, pp. 27-37, Jan 2002.

[4] F. Farag, C. Montoro and M. Schneider, "Digitally programmable switched-current FIR filter for low-voltage applications", IEEE J. Solid State Circuits, Vol. 35, pp. 637-641, Apr 2000.

[5] S. Mahmoud, M. Hashiesh, and A. Soliman, "Low-voltage digitally controlled fully differential current conveyor" IEEE Trans. Circuit and System-I, Vol. 52, pp. 2055-2064, Oct 2005.

[6] S. Brigati, F. Francesconi and M. Poletti, "A 147-dB dynamic range electronic attenuator for audiometric applications with on-chip 1-W power amplifier", IEEE. J. Solid State Circuits, Vol. 36, pp. 1087-1093, Jul 2001.

[7] C. Kuratli and Q. Huang, "A CMOS ultrasound range-finder microsystem", IEEE J. Solid State Circuits, Vol. 35. pp. 2005-2017, Dec 2000.